PROJECT PROFILE

2A701: Parasitic extraction and optimization for efficient microelectronic system design and application (PARACHUTE)

EDA FOR SOC DESIGN AND DFM

Partners:

Airbus
Alcatel
AMIS
Atmel
CONTI
EADS
Freescale
Infineon Technologies
iRoC Technologies
Philips
Robert Bosch
STMicroelectronics
Uni Balearic Islands (UIB)
Uni Madrid (Carlos III)
Uni Grenoble/TIMA
Uni Paderborn
Zuken

Project leader:

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Key project dates:

Start: January 2005
End: March 2009

Countries involved:

Austria
Belgium
France
Germany
The Netherlands
Spain

In the past two decades, advances in integrated circuit performance have been driven mainly by developments in semiconductor technology, whereas improvements in performance of electronics systems have been propelled or limited principally by the design methods employed. This has led to an increasing gap in terms of reliability, especially that caused by parasitic effects. To reduce this gap, the MEDEA+ PARACHUTE project is developing top-down extraction, modelling and analysis, and design methods linking device and systems development more strongly than ever before. The resulting reliability improvement will help place the European electronics industry at the forefront of global competition.

Reliability problems caused by both internal and external parasitic electromagnetic effects are an increasing concern for the mainstream electronics market, as they are amplified dramatically with the introduction of each new generation of ever smaller CMOS devices. For zero-fault applications such as safety-critical functions in cars or aircraft, these problems are daily ever more difficult to handle and a united overall effort has to be made for the future. Moreover, availability problems caused by these effects are increasingly worrying in telecommunications and even consumer electronics equipment.

Electromagnetic compatibility consideration of individual components is not sufficient; the electromagnetic reliability (EMR) of whole systems must be ensured, requiring co-design through inter-disciplinary cooperation that covers research, design and verification. The MEDEA+ 2A701 PARACHUTE project is therefore setting out to develop an innovative integral design approach and the necessary models, algorithms and tools that take into account all levels – integrated circuit (IC), IC package, high density packaging (HDP), high density interconnect (HDI) and printed circuit board (PCB) – to allow application optimisation in the context of electromagnetic interferences and particle radiation.

This MEDEA+ project brings together a large consortium that includes major European chipmakers, electronic systems designers, systems users and members of two key research groups: the 'new techniques and methodologies for particle radiation effects in microelectronic applications' R&D cluster and the 'future EMC/RF-modelling and simulation methodologies' competence network. The overall objective of PARACHUTE is to improve the electromagnetic reliability of applications based on nanometre circuits, microelectronics, microsystems technology and power electronic systems.

Integral top-down approach

Current design solutions to handle natural and artificial disturbances in combination with parasitic effects focus on optimisation of technology rather than analysis at various design levels such as cells, intellectual property (IP) blocks, IC applications, IC package, high density system structure, subsystem or even product level. Moreover,

existing design solutions have not yet been optimised because they lack an integral top-down overview and the integral analysis necessary to optimise the application.

PARACHUTE takes an integral top-down investigation and implementation approach using 'design-to-noise margin' (DNM) methodology. This methodology involves assuring the correct operation of an electronic device or system by proper setting of:

* Design parameters in the preceding hierarchy level – such as IC needs fulfilling certain design constraints to ensure system operation; and
* All related physical parameters within the same hierarchy level – for example, reduced crosstalk must not lead to increased electromagnetic emission.

The top-down approach covers three design hierarchies: application system – HDP/HDI level; IC package – system in package (SIP); and silicon chip – system on chip (SoC); together with the system concept and architecture choices.

This work targets electromagnetic emission (EME); electromagnetic susceptibility (EMS) – conducted, radiated and impulses – and natural particle sensitivity (SEU/SET); and signal (SI) and power (PI) integrity, and close proximity coupling effects. All these types of noise disturb functionality, reduce performance and decrease reliability of electronic systems. Therefore design needs to consider the noise level over the whole electronic system, including the chips used together with the IC package, silicon and, if necessary, additional passive components.

Research and implementation in PARACHUTE is driven by design challenges at the module level to keep the signal-to-noise ratio high enough to ensure proper operation and reliability. The design-to-noise margin is evaluated from the system level through the HDP/HDI level down to chip level at the 130 nm half pitch and below.

Since the focus in the MEDEA+ project lies on chip representation, module and package levels, all physical effects are treated at those design levels. At chip level, the research and implementation focus is on electromagnetic and particle effects. On-chip signal and power integrity issues such as crosstalk and substrate coupling are being handled predominantly in the parallel MEDEA+ ROBIN project. As these chip-level signal integrity issues will be investigated there, no related efforts are planned in PARACHUTE.

Three-stage approach

The PARACHUTE investigation-and-implementation approach covers three stages:

1. Investigation of physical effects;
2. Implementation of detection and design hardware, software and measurement setups; and
3. Validation of the mastering of physical effects in hardware and software.

These stages are reflected in the work package structure. Physical effects are investigated thoroughly in work packages one to three. Hardware test vehicles, simulation models, design flows and reliable measurement setups will be delivered by work packages four to six. Work package four provides the required hardware test vehicles, work package five the models and simulation software as well as design flows for noise minimisation and work package six the required measurement setups for product characterisation – some of which should result in new international standards.

Work package seven will use the results and the design and simulation methodologies from the other work packages to validate product sign-off. Hardware circuits, simulation and design methodologies and tools will be verified by measurement setups for successful cosmic noise sensitivity reduction on products and the maintenance of the necessary design-to-noise margin along the design-level hierarchy.

Promoting conceptual change

Success in PARACHUTE should initiate a conceptual change in dealing with induced physical noise in nanometre circuits in the European semiconductor development and systems application community, linking microelectronics design and systems development more strongly than ever before.

Particular emphasis will be given to the automotive sector as ever higher amounts of subsystems have to be integrated, to aerospace where the complexities of critical electronic systems are increasing rapidly, to consumer electronics, particularly body-wear microelectronics and wireless networks, and medical systems such as new lifestyle and personal healthcare products.

Availability of new design methodologies to handle electromagnetic and particle radiation parasitic effects and improve system reliability will reduce time to market and help to place these key European industrial sectors at the forefront of international competition.

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MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.